REMARKS

The examiner rejected claim 1 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 2 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a switching device between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 4 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 5 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 7 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a bipolar transistor between a

positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 8 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 9 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a switching device between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 11 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 12 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 14 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a bipolar transistor between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 15 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software

application may be used to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 16 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a switching device between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 18 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 19 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 21 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a bipolar transistor between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 22 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software

application may be combined to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 23 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a switching device between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 25 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 26 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 28 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU and a software application may be combined to dynamically control a bipolar transistor between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 29 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 30 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a switching device between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 32 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 33 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 35 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a PMU is used to dynamically control a bipolar transistor between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 36 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control power applied to a memory array based on application behavior.

The examiner rejected claim 37 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a switching device between a negative

terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 39 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a bipolar transistor between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 40 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a switching device between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 42 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162 and U.S. Patent No. 5,719,800. This rejection is respectfully traversed. There is no suggestion in either Houston or Mittal et al. to indicate that a software application may be used to dynamically control a bipolar transistor between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 3 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU and a software application may be combined to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 6 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al.

to indicate that a PMU and a software application may be combined to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 10 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU may be used to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 13 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU may be used to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 17 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a software application may be used to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 20 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a software application may be used to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 24 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al.

to indicate that a PMU and a software application may be combined to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 27 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU and a software application may be combined to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 31 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU may be used to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 34 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a PMU may be used to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

The examiner rejected claim 38 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al. to indicate that a software application may be used to dynamically control a MOSFET between a negative terminal on an on-chip cache memory array and GND of a power supply based on application behavior.

The examiner rejected claim 41 under 35 U.S.C. 103(a) as being anticipated by U.S. Patent No. 5,615,162, U.S. Patent No. 5,719,800, and U.S. Patent 6,498,762. This rejection is respectfully traversed. There is no suggestion in either Houston, Mittal et al., or Noda et al.

to indicate that a software application may be used to dynamically control a MOSFET between a positive terminal on an on-chip cache memory array and VDD of a power supply based on application behavior.

It is respectfully believed that none of the prior art of record either individually or in combination teaches the present invention as currently recited in claims 1-42. For the foregoing reasons, this application is respectfully believed to be in condition for allowance and such action is earnestly solicited at the Examiner's earliest convenience.

Respectfully submitted,

By_____

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